REMARKS

The present Amendment is in response to the Office Action having a mailing date of June 17, 2004. Claims 1-19 are pending in the present Application. Claims 1-19 are rejected. Claims 13 and 15-19 have been amended for clarity. Consequently, claims 1-19 remain pending in the present application. Applicant includes a Petition for Extension of Time to extend the deadline for filing a response by one (1) month from September 18, 2004 to October 17, 2004.

Present Invention

An application specific integrated circuit (ASIC) is disclosed. The ASIC includes a standard cell. The standard cell includes a plurality of logic functions. The ASIC also includes at least one bus coupled to at least a portion of the logic functions and a plurality of internal signals from the plurality of logic functions. Finally, the ASIC includes a filed programmable (FP) function coupled to the at least one bus and at least a portion of the plurality of internal signals. The FP function provides access to internal signals for observation and control.

An ASIC using a filed programmable gate array (FPGA) function within a standard cell design is utilized to create an internal-to-the-ASIC bridging of internal signals to observe and control of the internal signals of the ASIC. By the placement of the logic, which expresses a test program into the FPGA function and manipulates the I/O pins and/or other functional entities of interest, the ASIC function and/or surrounding logic can be easily verified. In addition, through this system, internal and/or system (external-to-the ASIC) conditions can be observed. Furthermore, a sequence of resets to different functional blocks can be executed utilizing a system and method in accordance with the present invention. Finally, through this system the

end user of the ASIC could write their own error condition correction FPGA code which would communicate using protocols of the existing system error condition architecture.

Claim Rejections-35 USC 103

The Examiner states,

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salem et al. U.S. Patent No. 5,844,917 in view of Laberge et al. U.S. Patent No. 6,012,148.

As per claim 1, Salem et al teach an adapter card with an application specific integrated card (ASIC) a field programmable gate array (FPGA) and program logic device (PLD), i.e., gate array logic. The PLD communicates with the system over I/O bus. The system can also communicate directly with FPGA via I/O bus. Test controls are sent from the FPGA to the ASIC. Data is scanned into the ASIC, and scanned out of the ASIC. The PLD and FPGA each contain one or more programmable options select (POS) registers. The FPGA also contains a scan state machine and a self-test state machine. (Fig. 2, column 2 lines 39-52) Not explicitly disclosed is that the contents of this test cards are located on a single ASIC.

However, in an analogous art, Laberge et al. teach that as today's computer systems are continually enhanced with respect to speed and computing power, the intricate nature and complexity often increases in parallel. To maintain a high degree of reliability in such systems, error processing is used to locate, report, and act on system faults and faults within particular components within the system. Scan testing is often used for custom VLSI chips and ASICs, because the internal signals simply are not accessible. Scan methods considers any digital circuit to be a collection of registers or flip-flops interconnected by combinatorial logic where test patterns are shifted into a large shift register organized from the storage elements of the circuit (column 1 lines 11-33). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the system of Salem et al. on a single ASIC. This would have been obvious as suggested by Laberge et al. (column 1 lines 13-19). To maintain a high degree of reliability in such systems, error processing is used to locate, report, and act on system faults and faults within particular components within the system. Error processing is important during the real-time execution of the computer system, but is also important during system test.

As per claims 2-4, Salem et al. teach the use of multiplexers as a connection for signals through programmable devices used in order to test the logic (column 2 lines 43-46, column 3 lines 5-8, and 25-34).

As per claims 5, 6, 12 and 14 based on test controls from the FPGA (one example of reconfigurable logic) to ASIC, test data is provided to the ASIC. The test data is then operated on

within the ASIC to exercise the one or more logic functions of the ASIC. Finally, a determination is made as to whether the output data from the ASIC contains any errors based on the software (figure 10, column 4 line 62 through column 5 line 7).

As per claim 7, Laberge et al. teach an error detection and recovery apparatus for monitoring, and recovering from, errors in a system having one or more logic units.

Abstract

As per claims 8, 9, 13 and 15, Laberge et al. teach that a microsequencer can recover from error. The microsequencer receives the particular error signal via bus, which provides the error A, error B through error n signals from the error A field. The ability for the microsequencer to read the error register allows the microsequencer to perform error analysis, as it therefore knows the particular error that occurred. The microsequencer includes recovery routines which can be stored at the microsequencer itself, or alternatively in a separate memory device. These microcode recovery routines are prepared in advance and written to properly recover from an error presented to the microsequencer. A microcode recovery routine can be triggered in response to a particular error. Using recovery code allows a test to continue to run despite the fact that known hardware problem exists. Furthermore, this also allows known hardware problems to be corrected without having to correct defective hardware in a custom chip (column 7 lines 28-61 Figure 2).

As per claims 10, 11, 18 and 19, Laberge et al. teach that a support controller may itself monitor a particular unit, or may act on a reported error originating from a particular unit or "watchdog" hardware/software component, which monitors for specific faults and reports them to the support controller. (Column 1 lines 45-49)

As per claims 16 and 17, Laberge et al. teach I an error detection and recovery circuit for monitoring for system errors. The system may include one or more individual logic units that together makes up the complete system. An error detection mechanism is provided to detect the errors in any of the logic units, and to provide error signals to indicate which of the logic units had an error and what error occurred. A first error recovery mechanism receives the error signals, and can perform a system-level recovery based on the particular error that occurred. A second error recovery mechanism also receives the error signals, and can perform a unit-level recovery. The error history is recorded from the bus history analyzer. (Column 3 lines 4-49)

Applicant respectfully disagrees.

Prior Art

Salem et al. (5,844,917)

An adapter card in a computer system includes an application specific integrated circuit (ASIC) and a filed programmable gate array (FPGA) coupled to the ASIC. Random data is provided to the ASIC logic function(s) by control of the FPGA, which is configured by a programmable logic device on the card and coupled thereto. The logic function(s) of the ASIC

is then exercised with the random data, and the output is compared with expected output by the system to determine if there are any errors. The determination is made based on a signature produced by a multiple input shit register (MISR) within the ASIC, based on the output data from the logic function(s). The FPGA can then be reconfigured for normal adapter card functions.

Laberge et al. (6,012,148)

An error detection and recovery apparatus for monitoring, and recovering from, errors in a system having one or more logic units. An error detector detects errors in the logic units, and provides error signals in response. A first error processor receives selected error signals, and performs system recovery according to the particular error signals present. A second error processor receives other selected error signals, and performs error recovery of the logic unit only, without affecting the rest of the system. The second error processor performs error recovery through real-time execution of error recovery routines at the logic unit. A selector is provided to determine which of the error signals are provided to the first and second error processors. A memory stack having multiple memory locations is also provided to store bus information captured from a bus, which can be used by the second error processor in its error recovery.

Discussion

Applicant submits that neither Salem et al. nor Laberge et al. singly or in combination teaches or suggests the present invention. Specifically, as has been above noted, the present invention is directed towards the ASIC which includes the standard design in which the FPGA function is incorporated within a standard cell design. This is accomplished by utilizing a field

programmable function coupled to at least a portion of the plurality of internal signals from the plurality of logic functions. In so doing, the logic functions can be monitored internally and the full perimeter functions provide access to the internal signals for observation and control. Salem shows a FPGA coupled to an ASIC where the ASIC can scan in and scan out information and the FPGA can provide test control information to the ASIC. However, there is no teaching in Salem that their signals internal to ASIC are observed and controlled as in the invention, as recited in claim 7. In Salem as above-mentioned, the FPGA does not access internal signals of the ASIC it actually receives external signals from the ASIC.

Laberge, although describes an error recovery mechanisms, neither teaches nor suggests the internal signals of the logic function for providing such observation and control. The combination of Salem and Laberge would provide for an adapter card that utilizes an ASIC which includes an error recovery mechanism. There is no teaching within any of these references for the use of any internal signals within the ASIC to be accessed by the field programmable function for observation and control.

Accordingly, claim 1 is neither taught nor suggested by the cited references.

Claims 2-12 are also allowable because they depend from an allowable base claim. Furthermore, neither Laberge nor Salem either singularly or in combination disclose a signal connector function which is in communication with a logic that selects the appropriate internal signal for observation and control.

Independent claims 13 and 15 have been amended to recite that the field programmable function monitors internal signals from the plurality of logic functions. As before mentioned, neither of the cited references singly or in combination teach this feature. Accordingly, applicant submits that claims 13 and 15 are allowable over the cited references. Accordingly claims 15,

16-19 are allowable since they depend upon an allowable base claim. Accordingly, Applicant respectfully requests reconsideration and allowance of claims 13-19 as now presented.

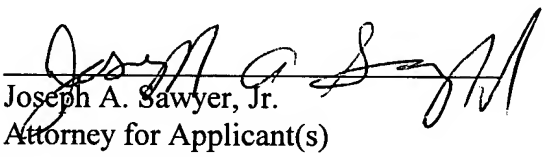
Accordingly, Applicant respectfully submits that claims 1-19 are now all in allowable form. Consequently, allowance and passage to issue of claims 1-19 of the present application are respectfully requested.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

SAWYER LAW GROUP LLP

October 14, 2004
Date



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